October 2004 Report of the Tevatron BPM Upgrade
wbs item 1.4.5.4 of the Run 2 Luminosity Upgrade Project
Bob Webber, Stephen Wolbers
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Project Manager's Summary:

The major areas of progress in October include accelerated delivery and testing of electronics and components, final specifications and bids for the timing and filter boards, final preparation of service buildings, progress on understanding Echotek board setup, filtering, and processing, and serious discussion/preparation for commissioning when the beam returns in late November. The order for the timing and filter boards will not provide production boards in time for first commissioning. A plan to adjust to this while not slowing down the system commissioning is being developed.

By the end of October deliveries of components included a total of 136 Echotek boards (of 150 ordered for the TeV BPM project), 600 matched pairs of analog filters (out of 600), cables, air dams for the VME crates, and two prototype cable panels for use above and below the VME crates. The Echotek boards have been tested using a modified version of the "Prep" test that was used to test similar boards used in the Recycler BPM system. Those boards that did not pass the tests are being studied for possible hardware or other problems and will be returned to Echotek for replacement if found to be unacceptable. This investigation is ongoing.

A 10% sample of the analog filters was tested against the documented specifications. Some of the filters were not within the nominal specifications for phase matching across the frequency spectrum. The variation from the specification is not large and was normally near the edges of the frequency band. This is not felt to be an issue with respect to position measurement and continues to be studied.

Both the timing and filter board designs were finalized and approved for fabrication. Bids were prepared and sent out on October 22. The bid period is two weeks at which point a better idea of final delivery schedules will be known. Given the expected schedule for the beam to return (late November) and the pace at which the systems can be commissioned a plan has been prepared to start commissioning with a mix of prototype and production electronics in the service building A3. To commission the next set of service buildings will likely require additional prototype boards. Prototype timing boards exist for the first 4 buildings. But special prototype filter boards will need to be built for the second through fourth service buildings. These are designed and can be built quickly and cheaply while allowing the critical components (filters) to be removed and placed on the production filter boards later.

Detailed commissioning plans are being formulated. This includes plans for the order of commissioning the service buildings as well as establishing a baseline for functionality and producing detailed plans for providing that functionality. The proposed plan is to

commission the A3 service building followed by B3,C3,D3,E3,F2, then B0 and D0, then A2, B2, C2, D2, E2, A4, B4, C4, D4, E4, A1, B1, C1, D1, E1, A0, F3, F4, F1.

Both the front-end of online software are advancing. 500 Hz of closed orbit measurements have been achieved with 6 boards in a crate, turn-by-turn capability now exists, diagnostics are being developed, and the online system is being readied for the transition from the old TeV BPM to the new TeV BPM system.

Much work was done in October to understand the Echotek board capabilities, how to test those capabilities and make relevant measurements, and to make decisions on how to set up and run the system when the beam returns in late November. This work will necessarily expand and intensify as we approach the date when beam returns.

Resources Used in October 2004:

The total number of FTE-months devoted to the project in calendar October 2004 from the Computing Division was reported to be 10.5 FTE-months with 25 people contributing. The total number of FTE-months devoted to the project from the Accelerator Division was 1.1 FTE-months with 5 people contributing. The total effort from both Divisions was 11.6 FTE-months. The following table gives the estimated or reported effort for both divisions (in FTE-months) since August of 2003.

Month	AD Effort	CD Effort	Total Effort
August, 2003	1.2	2.3	3.5
September, 2003	1.4	4.1	5.5
October, 2003	5.4	6.0	11.4
November, 2003	1.6	5.0	6.6
December, 2003	1.4	4.4	5.8
January, 2004	1.7	5.1	6.8
February, 2004	2.3	6.7	9.0
March, 2004	2.1	7.6	9.7
April, 2004	2.0	7.7	9.4
May, 2004	1.4	8.3	9.7
June, 2004	1.6	8.7	10.3
July, 2004	2.0	8.1	10.1
August, 2004	1.5	8.0	9.5
September, 2004	2.3	8.4	10.7
October, 2004	1.1	10.5	11.6
SUM (through Oct)	29.0	100.9	129.9

The effort is consistent with the wbs estimates of approximately 10-12 FTE per month during this period. The effort listed here is productive time worked and does not include vacation, sick leave, holidays, etc.

Purchase requisitions/procard obligations in October, 2004:

Fabrication bids for the timing and filter cards have been placed.

PRN56416 10/29/04 Grommets-Digikey 2500 $77.31 Monthly Total $77.31

Milestones:

The project had no milestones in October.

Meetings held, Reports Given:

Meetings were held in October on the following dates:

Project Meetings: October 6,11,13,14,20,21,27,28

Documents:

The following documents were written and added to the Accelerator Division Document Database in October:

Beams-doc-1381-v6 Echotek Board and Other Hardware Testing Status Timothy J. Kasza 28 Oct 2004

Beams-doc-1414-v2 First Echotek readout with the "envelope" filter Gustavo Cancelo 25 Oct 2004

Beams-doc-1421-v1 TeV BPM Commissioning Modes Jim Steimel 22 Oct 2004

Beams-doc-1407-v2 Echotek test bench studies Jim Steimel 22 Oct 2004

Beams-doc-1418-v1 Lark Filters Phase Matching Charts Timothy J. Kasza 20 Oct 2004

Beams-doc-1383-v3 TeV BPM Analog Board PRR Bob Forster *et. al.* 18 Oct 2004

Beams-doc-1413-v1 Echotek Update Eric James 16 Oct 2004

Beams-doc-1406-v3 TeV BPM Upgrade: Dependence of Position and Resolution on Intensity Robert K Kutschke 14 Oct 2004

Beams-doc-1384-v1 TeV BPM Analog Board Test Results Bob Forster *et. al.* 07 Oct 2004

Beams-doc-1397-v1 Analog filter testing results for TeV BPM Upgrade Timothy J. Kasza 07 Oct 2004

Subproject Leader Reports:

Electronics: Vince Pavlicek

The electronics group supported the continuing testing and investigation efforts in the testing area in FCC3. Simulation efforts aimed at understanding the Echotek signal processing continued progress toward the production Echotek algorithm. Production cables, Echotek modules, analog filter pairs and air dams are 90% in house and QC test procedures are being applied to all the parts or to sample sets. Some filters and Echotek modules did not meet the acceptance specifications. For the filters, we knew our initial acceptance criteria were restrictive and because the failing parts were just outside the criteria, we will relax the acceptance specifications less than 5% and include most of the outliers. More discussion of specific filters will continue. The Echotek modules have some errors that appear to come and go so we began extra testing to determine whether they are real hardware problems.

Upgraded firmware for the sub rack monitoring hardware is still pending.

Timing card and Filter card designs passed testing and Production Readiness Reviews and bid packages were prepared and sent out. Bids close 8 Nov. On the Timing Generator and Fanout card the initial testing of the TClk decoder was successful and now support for back-to-back TClk interrupts is being added and tested. Also a scheme for time tagging the data based on accelerator clocks was designed and is being implemented in the TGF firmware.

The production filter boards are not expected to arrive before the shutdown. To allow some commissioning to start with the beam startup at the end of November, a new temporary filter board was designed to provide 32 channels of inexpensive and simple filters using sockets to hold the Lark filters so they can easily move to the production boards later. The decision to produce these will depend on the delivery date given for the production filter cards.

Long lead-time items for analog module and timing module production are 100% in house.

Front-end/DAQ software: Margaret Votava

There has been significant progress during the month of October. The first important milestone was the achievement of the required readout rate of 500Hz in closed orbit mode. The turn-by-turn mode has been addressed and the diagnostics application is moving forward. A few problems have been addressed; there has been minor code restructure and discussions about timestamps.

The system is now capable to run the closed orbit mode in the required rate of 500Hz with the full crate (6 EchoTek boards). At this rate the processor has between 15% to

20% of time available for additional processing (e.g. calculate positions and apply calibration constants) The boards have been configured to select a single point for each measurement and the point is read using a single VME read. No DMA operation is required. Additionally some system tasks now have the priority set to a lower value than the TBPM tasks to avoid any interference. Most tasks have the priority changed at startup, while the shell task must have its priority changed after the crate has initialized.

The turn-by-turn mode has been added to the system. Currently it is possible to enter the turn-by-turn mode either by the W25 online application or through the front-end command line. Automatic turn-by-turn mode switch can be easily integrated. When the system switches to turn-by-turn mode the timing board is configured and a new configuration is loaded to the EchoTek boards. The data is read out from the six EchoTek boards through DMA chaining. It takes approximately 80ms to read out all data from 8K turns from a single board. Data from a turn-by-turn measurement is available for online read requests and also available to the diagnostics page. For diagnostics the application returns the points acquired for the first turn of the measurement, which contains a number of points equivalent to the burst count set in the EchoTek configuration file. An additional buffer specific for the turn-by-turn measurement has been added to the EchoTekPool class, allowing the system to quickly return to closed orbit mode. While the system is back in closed orbit mode the turn-by-turn buffer will be processed.

The raw ADC diagnostics mode has been implemented and is integrated to the diagnostics application. Data is available only to the W25 application. The acquisition delays, excluding the individual channel delays, can now be changed through the diagnostics application. The channel delays are already being sent to the front-end, but are not being sent to the EchoTek boards yet. This may require the re-initialization of the boards.

The missing interrupt from the timing problem has been detected and fixed. A unit test for testing basic functionality of the timing board hardware is in development. The test probes registers, checking written values, verifies the presence of BSYNC and TCLK signals. Also checks if the start and turn BSYNC events are received and if interrupts can be generated.

The new TCLK functionality in the timing board required some software changes. It differs from the recycler TCLK scheme, using only one interrupt vector, while the recycler uses one for each TCLK. Additional handshake between the software and the board is needed. The TCLK is not fully operational; we are working with the Electronics group to conclude the work.

There have been some discussions about handling timestamps in the system. There is the need of two types of timestamp. One coarse and one fine. The first one would be used for closed orbit measurements and for operations that do not require a very precise timestamp, while the second would be used in the turn-by-turn mode. The fine grain timestamp will be generated the timing board and will be controlled by specific BSYNC events and will be used by the processor to calculate the timestamp of each point within

the measurement. The coarse grain timestamp will use the clock provided by the processor, which is synchronized using the TCLK 0x8F.

Worked on and understood the bad ADC problem: a few (~4 out of 70) boards have bad ADCs -- In the ADC code probability/differential non-linearity distribution histograms, even numbered codes have twice of the expectations while odd codes have 0 entries. This problem happens every time when we run the tests. It is understood to be caused by stuck/missing ADC bit(s). The bad ADCs will be replaced.

Worked on the "random" noise problem and traced the root to the FPGA firmware (very likely): out of the 4 pilot boards, one could never pass the PREP tests because there were always one or two channels with a lot of random noise. The noise problem did not stay with any channel(s), but rather move between channels from test to test (with power cycles in between). The same problem showed up in 4 of the ~70 production boards. Re-testing the PREP "good" boards with repeated power cycles revealed that a previously "good" board can also get this kind of random noise after a few power cycles!

Once the noise shows up with a certain channel, there is indeed some pattern in the way the raw counts are corrupted: it seems the raw counts can not take certain values (bits), whenever a certain value (bit) is desired, we get always the same wrong value (bit). This clearly indicates a problem in the digital path, instead of the analog part. Since the same channel can be either good or bad after a power cycle, we believed that the FPGA initialization after power up may not be done consistently/properly. Contacted Ed of Echotek, they see the same problem a few times. Ed is working on it -- a firmware update is certainly necessary. Mark B believes there is 99% chance this problem will be fixed by a firmware update.

Online software: Brian Hendricks

During the past month the BPMUTI library has been modified to support the new frame types required by the upgrade. Two new database tables have been created to support SDA access to BPM data. One table maintains a version history of each house so that the mix of old and new houses on a given date can be reconstructed, and a correct BPM orbit can be constructed from the appropriate SDA data. A second table contains the mapping of SDA devices to frame types and numbers. The BPMUTI library has been updated to make use of both of these tables, and the SDA support has been completed. With this work, the VMS library support is essentially complete. However, as application work continues, there will undoubtedly be required modifications to the library code. On the application front, a meeting was held to spec out additional changes to the diagnostic and engineering application. One of these changes was the addition of a timer delay subpage. This subpage has been implemented. Other changes arising from the meeting are still in progress. The means for reading back crate status has not yet been resolved. Dawn is estimating that HTTP support will not be available till the first or second quarter of 2005. We are presently weighing our options which include using an RS232 interface or requesting UDP support from Dawn. This effort is ongoing.

Offline software: Rob Kutschke

This month I restarted the job of analysing data taken before the shutdown. The main project was the comparison of the data taken with an uncoalesced batch in the machine to data taken with coalesed bunches. A report is in preparation and will be ready in early November.

Hardware tracking/testing: Tim Kasza

Throughout the month of October, Echotek A/D boards continued to arrive at a weekly rate slightly ahead of schedule. Overall, 136 out of 150 boards have been delivered, tagged and entered into CD's equipment tracking database (equipdb). As the month progressed, our testing efforts focused toward understanding and classifying boards that were placed on hold during testing for several different performance issues. One issue was with a large percentage of boards that had one or more channels slightly failing the gain acceptance specification. After examining channel gain distribution across the first 42 boards, this issue was resolved by revising the gain specification slightly lower to between 0.875 and 0.945 (0.910 +/- 0.035). Echotek has been made aware and is investigating other issues that include boards with random channels that display bad raw ADC and channels that fail differential non-linearity. A resolution to these issues is currently pending from Echotek.

All 600 pairs of Lark filters have been delivered. Sample testing with data was completed on 10% of the filters pairs. Phase testing results revealed some filter pairs with readings slightly outside of the acceptance range. This is mainly at the edges of the 8 MHz frequency spectrum. Thus far, these results are not seen as an issue. One additional test was conducted on five previously tested filter pairs. This involved temperature baking filters at 53 degrees Celsius, cooling to room temperature and then retesting. The results indicated no significant changes.

Various other hardware items continued to arrive. All of the Air Dam cards, plus 316 of the six-foot to SMB cables with attached labels were delivered and placed in storage pending installation.

Progress in other areas includes the installation of parts that completed the upgrade of two early/prototype Dawn crates. Mounting rails for the Dawn crates were installed or at least placed in equipment racks in the remaining service buildings. Cable panels have been installed in A3 service building and will be used for trying out various cable connecting/routing methods.